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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,193	12/31/2003	Everett B. Lee	42.P18035	2545

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EXAMINER	
ERDEM, FAZLI	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
05/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/751,193	LEE, EVERETT B.	
	Examiner	Art Unit	
	Fazli Erdem	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-17 and 23-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-17 and 23-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments and Amendments

1. Applicant's arguments and amendments, filed 4/19/2007, with respect to the rejection(s) of claim(s) 12-17 and objections to the claims 23-26 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wu.

2. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "one-dimensional" in claim12 is used by the claim to mean "length much greater than the width", while the accepted meaning is "relating to a line." The term is sufficiently redefined in the specification on page 6 for the instant case.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 12-17 and 23-36 rejected under 35 U.S.C. 102(e) as being anticipated by Wu (6,765,258).

Regarding Claim 12, Wu discloses a stack-gate flash memory cell structure and its contactless flash memory arrays where in Figs. 3I(B), 4, and 5, it is disclosed a flash memory cell comprising: a plurality of gate stacks 314(b) formed on a substrate 300, and a plurality of active regions 309b formed in the substrate, wherein each of the plurality of the gate stacks has a gate stack length and a gate stack width; an interlayer dielectric (ILD) 317a deposited over the gate stacks and the active regions; a one-dimensional slot patterned across active regions 309b in Fig. 4 in the ILD, wherein the one dimensional slot is to provide access to the plurality of active regions; and a bit line CSBL0- CSBL1 formed in the single slot, wherein the bit line is to contact the plurality of active regions through slot, wherein the one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is the gate stack width. 13. (Original)

Regarding Claim 13, the flash memory cell of claim 12, wherein the bit line 309b/310 comprises a tungsten plug as disclosed in column 6 lines 8-25

Regarding Claim 14, wherein the flash memory cell is a NOR memory cell.

Regarding Claim 15, plurality of nitride spacers 308 are adjacent to the gate stacks.

Regarding Claim 16, in Fig. 3I(b), control gates are 314b and floating gates are 302c

Regarding Claim 17, in Fig. 4, the word lines are labeled WL0 and they care in contact with the control gate.

Regarding Claim 23, Wu discloses a flash memory device where in Figs. 3I(b) and 4 it is disclosed a plurality of gate stacks 314(b) formed on a substrate, wherein an etch stop layer 313 in Fig. 3I(a) a forms a top surface of each gate stack within the plurality, a plurality of active regions 309b formed in the substrate; an interlayer dielectric (ILD) 317a deposited on the plurality of gate stacks and on the plurality of active regions; a one-dimensional slot patterned across active regions 309b in Fig. 4 patterned in the ILD providing access to the plurality of active regions; and a bit line formed in the slot, the bit line in contact with the top surfaces of the gate stacks and in contact with the plurality of active regions.

Regarding Claim 24, wherein the bit line 309b/310 comprises a tungsten plug as disclosed in column 6 lines 8-25.

Regarding Claim 25, in column 8 lines 26-48, the required silicide layer is disclosed.

Regarding Claim 26, layers 313 in Fig. 3I(a) is a dielectric layer.

Regarding Claim 27, layer 313 is nitride layer.

Regarding Claim 28, layer 315a in Fig. 3I(b) which can be considered as an etch stop layer is a silicide layer.

Regarding Claim 29, a nitride spacer 308a is adjacent to each of the plurality of gate stacks.

Regarding Claim 30, in Figs 3I(a), 3I(b) and 4, Wu disclose a nonvolatile memory device comprising: a plurality of gate stacks 314b formed on a substrate 300, wherein each gate stack within the plurality comprises an etch stop layer 313 and 315a; a plurality of active regions formed 309b in the substrate; an interlayer dielectric (ILD) 317a on the plurality of active regions and on and adjacent to each gate stack of the plurality of gate stacks and; bit line

BL0/309b (in Fig. 4) formed in a slot, the bit line in contact with the etch stop layer of the plurality of gate stacks and in contact with the plurality of active regions.

Regarding Claim 31, wherein the bit line 309b/310 comprises a tungsten plug as disclosed in column 6 lines 8-25.

Regarding Claim 32, in column 8 lines 26-48, the required silicide layer is disclosed.

Regarding Claim 33, etch stop layer 313 is a dielectric layer.

Regarding Claim 34, etch stop layer 313 is a nitride dielectric layer.

Regarding Claim 35, etch stop layer 315a is a silicide layer.

Regarding Claim 36, spacers 308a are located adjacent to each of the plurality of gate stacks.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (571) 272-1914. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FE
May 3, 2007

SUE A. P[illegible]
SUPERVISORY PA[illegible] EXAMINER